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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 200
TROY, MI 48098

EXAMINER
HSU, JONI

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,485	BOOTH, LAWRENCE A.	
	Examiner	Art Unit	
	JONI HSU	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see p. 8, filed June 27, 2007, with respect to 35 U.S.C. 112 rejection have been fully considered and are persuasive. 35 U.S.C. 112 rejection of Claim 9 has been withdrawn.

2. Applicant's arguments, see p. 9-12, filed June 27, 2007, with respect to rejection(s) of claim(s) 1, 3-9, and 11-15 under 35 U.S.C. 103(a) have been fully considered and are persuasive. So, rejection has been withdrawn. However, upon further consideration, new ground(s) of rejection is made in view of Saito (US005774134A).

3. Applicant's arguments filed June 27, 2007, with respect to Claims 16-22 have been fully considered but they are not persuasive.

4. As per Claim 16, Applicant argues cited references do not teach data from external frame buffer is copied to internal frame buffer during new frame refresh operation. New frame display refresh operation includes reading data by display controller from external frame buffer (p. 11).

In reply, Examiner respectfully points out Claim 16 does not specify that loading copy of display data from external frame buffer to internal frame buffer occurs during portion of new frame display refresh operation **that includes reading display data from external frame buffer**. Yoshikawa (US006393520B2) teaches reading display data from external frame buffer (14, Fig. 6) by display controller (13, 19) during new frame display refresh operation; and loading copy of display data from external frame buffer to internal frame buffer (12) during new frame display refresh operation (c. 9, ll. 57-67). Since Claim 16 does not specify that loading

occurs during portion of new frame display refresh operation **that includes reading display data from external frame buffer**, Yoshikawa is still considered to teach this limitation.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito (US005774134A), Yoshikawa (US006393520B2), Takala (US006909434B2), and Pope (US005847705A).

8. As per Claim 1, Saito teaches apparatus comprising display controller (24, Fig. 7); 1st frame buffer 23 coupled to display controller 24 (c. 5, ll. 42-55; c. 6, ll. 4-8). When storing image data of one frame is completed, image data is transferred from 2nd frame buffer (22) to 1st frame buffer (23), and, also, is directly provided for image output unit (20) (c. 5, ll. 49-52), which comprises display controller (24) (c. 5, ll. 56-60). As shown in Fig. 7, data is transferred from 2nd frame buffer (22) to 1st frame buffer (23), and, also, is directly provided for display controller

(24) (c. 5, ll. 49-60). Fig. 7 shows control circuitry (28) controls these transferring operations (c. 5, ll. 67-c. 6, ll. 4). So, Saito teaches control circuitry (28, Fig. 7) to copy display data from 2nd frame buffer (22) to 1st frame buffer (23) during reading of same display data by display controller (24) from 2nd frame buffer (22) (c. 5, ll. 49-60; c. 5, ll. 67-c. 6, ll. 4).

However, Saito does not teach second frame buffer is external frame buffer. However, Yoshikawa teaches apparatus comprising processing unit (13, Fig. 6) that decides which of frame buffers is being read or written (c. 9, ll. 16-18), and D/A converter (19) outputs video data to monitor from frame buffers (c. 9, ll. 25-28). So, processing unit and D/A converter are considered to be display controller. Yoshikawa teaches internal frame buffer (12) coupled to display controller (c. 9, ll. 6-8; c. 9, ll. 25-28); and control circuitry (15) to copy display data from external frame buffer (14) to internal frame buffer, wherein display data copied into internal frame buffer is same display data read by display controller from external frame buffer (c. 9, ll. 47-56; c. 7, ll. 11-15; c. 9, ll. 29-31, 58-67).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Saito so 2nd frame buffer is external frame buffer as suggested by Yoshikawa. Yoshikawa suggests in some applications, required storage capacity cannot be obtained by internal memory alone. So, external frame buffer is added, thereby obtaining desired storage capacity by using internal and external frame buffers in combination (c. 1, ll. 29-41).

However, Saito and Yoshikawa do not teach after display data is copied, same display data is located in internal frame buffer until new frame is available in external frame buffer. However, Takala teaches after display data is copied from external frame buffer (12, Fig. 1) to internal frame buffer (22), internal frame buffer is only updated after new frame is available in

external frame buffer (c. 2, ll. 1-19). So, after display data is copied, same display data is located in internal frame buffer until new frame is available in external frame buffer.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Saito and Yoshikawa so after display data is copied, same display data is located in internal frame buffer until new frame is available in external frame buffer as suggested by Takala. Takala suggests two frame buffers are needed. One frame buffer is integrated in display so display can be in mobile electronic device (c. 2, ll. 1-3). Other frame buffer is external frame buffer that is accessible by software so software can change contents of this frame buffer. External frame buffer is copied to integrated frame buffer to update display (c. 1, ll. 12-22), and so same display data is located in both frame buffers after display is copied. Integrated frame buffer is only updated when new frame is available in external frame buffer because this reduces amount of transferring of display data from external memory to internal memory since display data is not transferred when display contents are not changed, which reduces power consumption (c. 1, ll. 47-67; c. 2, ll. 1-19).

However, Saito, Yoshikawa, and Takala do not explicitly teach same display data is located in internal frame buffer and external frame buffer until new frame is available in external frame buffer. Takala teaches display data is transferred from external frame buffer to internal frame buffer (c. 1, ll. 12-22), however Takala does not explicitly teach display data remains in external frame buffer after it has been transferred. However, "transferring" data can mean data is transferred from one frame buffer to another frame buffer so there is copy of same data in each of frame buffers. This is taught in Pope, as Pope teaches display data is transferred from second frame buffer (18) to first frame buffer (20), and copy of display data remains in second frame

buffer after it has been transferred (c. 7, ll. 36-49). So, Pope teaches same display data is located in first frame buffer (20) and second frame buffer (18) until new frame buffer is available in second frame buffer (c. 7, ll. 36-49).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify internal (first) frame buffer and external (second) frame buffer of Takala so same display data is located in both frame buffers until new frame is available in second frame buffer because Pope suggests same display data needs to be maintained in both frame buffers so there is reference means for detecting changes in second frame buffer. Without first frame buffer as reference means for detecting changes in second frame buffer, it would be necessary for system to operate as if entire contents of second frame buffer were continuously changed. In that event, all memory locations of external frame buffer would be continuously updated, even in those memory locations where no display data change had occurred, resulting in substantial increase in overhead and degradation in system performance (c. 8, ll. 20-30). So, Pope suggests advantage of being able to compare contents of frame buffers so as to determine if contents are different at any corresponding memory locations, and only copying contents of changed memory locations to first frame buffer. Takala only teaches ability to detect when application updates second frame buffer (c. 2, ll. 1-19), and therefore must transfer entire contents of second frame buffer to first frame buffer since there is no way to detect which memory locations have changed since same display data is not stored in both frame buffers at same time. So, it would be advantageous to modify Takala with this teaching from Pope.

9. As per Claim 2, Saito teaches display data is copied into first frame buffer (23, Fig. 7) simultaneously with display controller (24) reading display data from second frame buffer (22) (c. 5, ll. 49-60).

However, Saito does not teach second frame buffer is external frame buffer. However, Yoshikawa teaches this limitation, as discussed in rejection for Claim 1.

10. As per Claim 3, Saito does not teach display controller reads display data from internal frame buffer until display controller receives signal indicating that external frame buffer contains most recent display data. However, Takala teaches reading display data from internal frame buffer (22, Fig. 1) until receiving signal indicating external frame buffer (12) contains most recent display data (c. 2, ll. 1-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Saito so display controller reads display data from internal frame buffer until display controller receives signal indicating that external frame buffer contains most recent display data because Takala suggests this reduces amount of transferring of display data from external memory to internal memory since display data is not transferred when display contents are not changed, which reduces power consumption (c. 1, ll. 47-67).

11. As per Claim 4, Saito does not teach display controller reads display data from internal frame buffer at least one time after new frame display refresh operation. However, Takala teaches reading display data from internal frame buffer (22, Fig. 1) at least one time after new frame display refresh operation (c. 2, ll. 1-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Saito so display controller reads display data from internal frame buffer at

least one time after new frame display refresh operation because Takala suggests it is advantageous for display data to be read from internal frame buffer for mobile devices and display data is read from internal frame buffer after new frame display refresh operation so display data that is read is updated display data (c. 1, ll. 6-24).

12. As per Claim 5, Saito does not teach display controller, internal frame buffer and control circuitry are disposed on single graphics chip and external frame buffer is disposed on another chip separate from graphics chip. However, Yoshikawa teaches display controller (13, 19, Fig. 6), internal frame buffer (12) and control circuitry (15) are disposed on single graphics chip (10) and external frame buffer (14) is disposed on another chip separate from graphics chip, as shown in Fig. 6. Data processor (1, Fig. 1) is a chip (c. 5, ll. 59-61). Fig. 6 shows video controller (10, Fig. 6), to which data processor of Yoshikawa's invention is applied (c. 9, ll. 5-8). So, video controller is one example of data processor of Yoshikawa's invention, and since data processor is a chip, this means that video controller is a chip.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Saito so display controller, internal frame buffer and control circuitry are disposed on single graphics chip and external frame buffer is disposed on another chip separate from graphics chip as suggested by Yoshikawa. Yoshikawa suggests that incorporating display controller, internal frame buffer and control circuitry on single graphics chip allows for data to be transferred at considerably high bit rate, because processing unit and internal frame buffer can be connected together via short data bus having broad bit width. According, high-speed data processing can be performed while making full use of performance of processing unit, which

makes it possible to provide smooth video images (c. 1, ll. 11-28). Advantage of having external frame buffer on separate chip (c. 1, ll. 29-41) was discussed in rejection for Claim 1.

13. As per Claim 6, Saito does not expressly teach display controller, internal frame buffer and control circuitry are disposed on single processor chip. However, Yoshikawa teaches display controller (13, 19, Fig. 6), internal frame buffer (12) and control circuitry (15) are disposed on single processor chip (10), as shown in Fig. 6. This would be obvious for reasons for Claim 5.

14. As per Claim 7, Saito does not teach control circuitry comprises register to hold at least one data transaction of display data. But, Yoshikawa teaches control circuitry 15 comprises at least one register 16 to hold at least one data transaction of display data (c. 9, ll. 52-56).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Saito so control circuitry comprises at least one register to hold at least one data transaction of display data because Yoshikawa suggests that this makes it possible to exchange data efficiently, while reducing overhead necessary for data exchange as much as possible, and data can be exchanged very fast and smooth (c. 9, ll. 65-c. 10, ll. 6).

15. As per Claim 8, Saito doesn't teach control circuitry generates write signal used by internal frame buffer based on external memory read signal, memory clock signal. But, Yoshikawa teaches control circuitry 15 generates write signal to be used by internal frame buffer 12 based on external memory 14 read signal and memory clock signal (c. 9, ll. 47-52, 56-67).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Saito so control circuitry is to generate write signal to be used by internal frame buffer based on external memory read signal and memory clock signal because Yoshikawa

suggests this enable control circuitry to control timing of data exchange so data is exchanged efficiently and quickly (c. 9, ll. 47-52, 56-67; c. 10, ll. 1-11).

16. As per Claim 9, Saito teaches system having processor (11, Fig. 6; c. 4, ll. 51-53); display device (21; c. 5, ll. 56-60); graphics processor (14, 15) coupled between processor 11 and display device (21) (Fig. 6; c. 4, ll. 51-58), graphics processor (14, 15) including display controller (20, Fig. 6; 24, Fig. 7) (c. 5, ll. 37-41, 56-57), 1st memory array (19, Fig. 6; 23, Fig. 7) (c. 5, ll. 37-44) and data copy circuitry (28) (c. 5, ll. 67-c. 6, ll. 4); and 2nd memory array (22) (c. 5, ll. 43-44), data copy circuitry (28) enables data from 2nd memory array (22) to be copied to 1st memory array (23) during an operation that includes reading of data by display controller (24) from 2nd memory array (22) (c. 5, ll. 49-60; c. 5, ll. 67-c. 6, ll. 4), as discussed for Claim 1.

However, Saito does not teach expressly teach graphics processor is graphics chip, second memory array is external memory array disposed on another chip separate from graphics chip, wherein data copy circuitry is coupled between external memory array and internal memory array. However, Yoshikawa teaches graphics processor is graphics chip (10, Fig. 6; c. 9, ll. 6-8, 16-18, 25-28), external memory array (14; c. 9, ll. 6-8) disposed on another chip separate from graphics chip, as shown in Fig. 6, wherein data copy circuitry is coupled between external memory array and internal memory array (c. 9, ll. 47-56; c. 7, ll. 11-15; c. 9, ll. 29-31, 58-67). This would be obvious for same reasons given in rejection for Claim 1.

However, Saito and Yoshikawa do not teach data from external memory array is copied to internal memory array during new frame display refresh operation, wherein after display data is copied, same display data is located in internal frame buffer until new frame is available in external frame buffer, and wherein subsequent display refresh operations are accomplished by

display controller retrieving data from internal memory array until new frame is available in external memory array. However, Takala teaches data from external memory array (12) is copied to internal memory array (22) during new frame display refresh operation, wherein subsequent display refresh operations are accomplished by retrieving data from internal memory array until new frame is available in external memory array (c. 2, ll. 1-19). After display data is copied from external frame buffer (12, Fig. 1) to internal frame buffer (22), internal frame buffer is only updated after new frame is available in external frame buffer (c. 2, ll. 1-19). So, after display data is copied, same display data is located in internal frame buffer until new frame is available in external frame buffer. This would be obvious for reasons given in rejections for Claims 1 and 3.

However, Saito, Yoshikawa, and Takala do not teach same display data is located in internal frame buffer and external frame buffer until new frame is available in external frame buffer. However, Pope teaches this (c. 7, ll. 36-49), as discussed for Claim 1.

17. As per Claim 10, it is similar in scope to Claim 2, and so is rejected under same rationale.

18. As per Claim 11, Saito teaches display data copied into 1st memory array (23) is same display data read by display controller (24) from 2nd memory array (22) (c. 5, ll. 49-60).

However, Saito does not teach second memory array is external memory array. However, Yoshikawa teaches this limitation, as discussed in rejection for Claim 1.

19. As per Claim 12, Saito teaches graphics generator (14a, Fig. 6) disposed on graphics processor (14, 15) (c. 4, ll. 54-67).

However, Saito does not expressly teach graphics processor is graphics chip. However, Yoshikawa teaches this limitation, as discussed in rejection for Claim 9.

20. As per Claims 13-14, these claims are similar in scope to Claims 7-8 respectively, so are rejected under same rationale.

21. As per Claim 15, Saito does not teach portable power source coupled to power display controller, internal memory array, external memory array and data copy circuitry. However, Takala teaches portable power source coupled to power (c. 1, ll. 59-62) the display (24, Fig. 1), internal memory array (22), and external memory array (12) (c. 2, ll. 1-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Saito to include portable power source because Takala suggests advantage of being able to use this display in mobile device (c. 1, ll. 59-62).

22. Claims 16-18 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (US006393520B2), Takala (US006909434B2), and Pope (US005847705A).

23. As per Claim 16, Yoshikawa teaches method comprising reading display data from external frame buffer (14, Fig. 6) by display controller (13, 19) during new frame display refresh operation; and loading copy of display data from external frame buffer to internal frame buffer (12) during new frame display refresh operation (c. 9, ll. 57-67).

However, Yoshikawa does not teach same display data is located in internal frame buffer until new frame is available in external frame buffer. However, Takala teaches this limitation (c. 2, ll. 1-19), as discussed in the rejection for Claim 1.

However, Yoshikawa and Takala do not teach same display data is located in internal frame buffer and external frame buffer until new frame is available in external frame buffer. However, Pope teaches this (c. 7, ll. 36-49), as discussed in rejection for Claim 1.

24. As per Claim 17, Yoshikawa does not teach determining if new frame is available in external frame buffer; and reading display data in internal frame buffer by display controller during subsequent display refresh operations if new frame is not available in external frame buffer. However, Takala teaches determining if new frame is available in external frame buffer (12); and reading display data in internal frame buffer (22) during subsequent display refresh operations if new frame is not available in external frame buffer (c. 2, ll. 1-19). This would be obvious for the same reasons given in rejection for Claim 3.

25. As per Claim 18, Yoshikawa teaches display data from the external frame buffer (14, Fig. 6) includes rendered graphics objects or an entire frame (c. 9, ll. 6-8, 25-28).

26. As per Claim 20, Yoshikawa teaches loading of data from external frame buffer (14, Fig. 6) to the internal frame buffer (12) is accomplished using data copy circuitry (15; c. 9, ll. 47-56).

27. As per Claim 21, Yoshikawa teaches disposing display controller (13, 19, Fig. 6), internal frame buffer (12) and data copy circuitry (15) on single graphics chip (10); and disposing external frame buffer (14) on another chip separate from graphics chip, as shown in Fig. 6. Data processor (1, Fig. 1) is a chip (c. 5, ll. 59-61). Fig. 6 shows video controller (10, Fig. 6), to which data processor of Yoshikawa's invention is applied (c. 9, ll. 5-8). So, video controller is one example of data processor of Yoshikawa's invention, and since data processor is a chip, this means video controller is a chip.

28. As per Claim 22, Yoshikawa teaches loading of data from external frame buffer (14, Fig. 6) to internal frame buffer (12) further comprises temporarily storing at least one data transaction of display data in register (16; c. 9, ll. 52-56); and writing stored data into internal frame buffer based on external memory read signal (c. 9, ll. 57-67).

29. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa (US006393520B2), Takala (US006909434B2), and Pope (US005847705A) in view of Saito (US005774134A).

Yoshikawa, Takala, and Pope are relied on for teachings discussed relative to Claim 16. Yoshikawa teaches reading data from external frame buffer by display controller and loading data from external frame buffer to internal frame buffer, as discussed in rejection for Claim 16.

However, Yoshikawa, Takala, and Pope do not teach reading of data from external frame buffer by display controller is executed simultaneously with loading of data from external frame buffer to internal frame buffer. However, Saito teaches reading of data from second frame buffer (22, Fig. 7) by display controller (24) is executed simultaneously with loading of data from second frame buffer (22) to first frame buffer (23) (c. 5, ll. 49-60), as discussed in rejection for Claim 1. So, Yoshikawa can be modified so reading of data from external frame buffer by display controller is executed simultaneously with loading of data from external frame buffer to internal frame buffer, as suggested by Saito.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Yoshikawa, Takala, and Pope so reading of data from external frame buffer by display controller is executed simultaneously with loading of data from external frame buffer to internal frame buffer because Saito suggests this increases transferring speed (c. 5, ll. 49-60).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628